REMARKS

In the interest of clarity, the Item Numbers below correspond to the Examiner's Item Numbers in the Office Action.

1. With this Response, Applicant cancelled Claims 23-25 and 76-81, by which Claims **1-22, 26-30** and **34** are pending, which Applicant will presently discuss.

2. The Examiner withdrew Claims 76-81 from consideration as being directed to a non-elected invention. Without prejudice to their future prosecution, Applicant cancelled Claims 76-81, for which Applicant reserves the right to pursue in a related application, but which presently renders moot the Examiner's Election/Restrictions.

3. The Examiner rejected **Claims 13-30** and **34** under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Respectfully, Applicant traverses and requests withdrawal.

As per Claim 13, the Examiner asserts the claim is indefinite. Respectfully, Applicant traverses and requests withdrawal. Nevertheless, Applicant amended Claim 13 to indicate the following: i) the phase detector comprises means for receiving CIN and CDLY; ii) the phase detector comprises means for outputting a pair of branches each having a logical level; and iii) the memory device comprises means for reducing a number of delay stages for a selected signal to pass through the SMD based on one of the plurality of conditions. Other minor changes were also made, such as specifying that the number of delay stages is reduced for the selected signal to pass through the SMD. Accordingly, Applicant respectfully asserts that Claim 13 is not indefinite, and requests that the Examiner withdraw the rejection.

As per Claims 14-17, the Examiner rejected these claims for the same reasons noted in Claim 13. Respectfully, Applicant traverses and requests withdrawal. More specifically, Applicant notes that since Claims 14-17 depend from Claim 13, and Applicant's belief that Applicant's arguments have successfully overcome the Examiner's rejection of Claim 13, any further rejection to Claims 14-17 is thereby obviated and rendered moot.

As per Claim 18, the Examiner rejected this claim for the same reasons noted in Claim 13. Respectfully, Applicant traverses and requests withdrawal. Nevertheless, Applicant amended Claim 18 to indicate the following: i) the phase detector comprises means for receiving CIN and CDLY; ii) the phase detector comprises means for outputting a pair of branches each having a logical level; and iii) the system comprises means for reducing a number of delay stages for a selected signal to pass through the SMD based on one of the plurality of conditions. Other minor changes were also made, such as specifying that the number of delay stages is reduced for the selected signal to pass through the SMD. Accordingly, Applicant respectfully asserts that Claim 18 is not indefinite, and requests that the Examiner withdraw the rejection.

As per Claim 19, the Examiner asserts that various recitations are misdescriptive, confusing, or unclear. Respectfully, Applicant traverses and requests withdrawal. Nevertheless, Applicant amended Claim 19 to indicate the following: i) the input buffer comprises means for receiving an external clock signal; and ii) the phase detector comprises first input means for receiving CIN, second input means for receiving CDLY, means for generating one of a plurality of output signal combinations, means for connecting a CDLY SMD input to the measurement delay line input, means for connecting a SMD output connected to the variable delay line output, and a circuit selectively inputting CIN or CIN' as a CIN SMD input based on the phase of the signals. Other minor changes were also made, such as specifying that the number of delay stages is reduced for the external clock signal to pass through the SMD. Accordingly, Applicant respectfully asserts that Claim 19 is not indefinite, and requests that the Examiner withdraw the rejection.

As per Claims 20-22, the Examiner rejected these claims for the same reasons noted in Claim 19. Respectfully, Applicant traverses and requests withdrawal. More specifically, Applicant notes that since Claims 20-22 depend from Claim 19, and Applicant's belief that Applicant's arguments have successfully overcome the Examiner's rejection of Claim 19, any further rejection to Claims 20-22 is thereby obviated and rendered moot.

As per Claims 23-25, the Examiner rejected these claims for the same reasons noted in Claims 13, 16, and 14, respectively. Respectfully, Applicant traverses and requests withdrawal. Nevertheless, Applicant has cancelled Claims 23-25.

As per Claim 26, the Examiner asserts the claim is indefinite. Respectfully, Applicant traverses and requests withdrawal. Nevertheless, Applicant amended Claim 26 to indicate the

following: i) the phase detector comprises means for receiving CIN and CDLY; ii) the phase detector comprises means for generating a plurality of output signal combinations; iii) the logic is in electronic communication with the phase detector; and iv) the system selectively feeds CIN or CIN' into the SMD. Other minor changes were also made, such as specifying that the number of delay stages is reduced for a selected signal to pass through the SMD. Accordingly, Applicant respectfully asserts that Claim 26 is not indefinite, and requests that the Examiner withdraw the rejection.

As per Claims 27-30, the Examiner rejected these claims for the same reasons noted in Claim 19. Respectfully, Applicant traverses and requests withdrawal. More specifically, Applicant notes that since Claims 27-30 depend from Claim 26, and Applicant's belief that Applicant's arguments have successfully overcome the Examiner's rejection of Claim 26, any further rejection to Claims 27-30 is thereby obviated and rendered moot.

As per Claim 34, the Examiner asserts that the functional recitation on the last four lines do not have any elements and/or structure to support. Respectfully, Applicant traverses and requests withdrawal. Nevertheless, Applicant amended Claim 34 to indicate the following: i) the phase detector comprises means for receiving CIN and CDLY; and ii) the logic is in electronic communication with the phase detector to select one of the output signal combinations corresponding to the timing conditions of the signals to input CIN into the SMD when $t_{mdl} > t_{ck}/2$ and input CIN' into the SMD when $t_{mdl} < t_{ck}/2$ to reduce a number of delay stages in the SMD. Other minor changes were also made, such as specifying that the second bus interconnects the memory controller to the plurality of memory devices. Accordingly, Applicant respectfully asserts that Claim 34 is not indefinite, and requests that the Examiner withdraw the rejection.

4. Applicant thanks the Examiner for considering Applicant's 10/23/03 arguments. As previously mentioned, Applicant cancelled **Claims 76-81**, obviating the need to respond to the Examiner's restriction/election requirement at this time.

5. The Examiner indicates Claims 1-12 are allowed, for which Applicant is grateful. In addition, Applicant added the word "and" in **Claim 10** for grammatical clarity.

6-7. Applicant believes that the amendments made to **Claims 13-30 and 34** will allow the Examiner to favorably re-consider these claims.

CONCLUSION

Applicant believes Applicant has overcome the Examiner's rejections of Claims 13-30 and 34. Moreover, Applicant believes that pending Claims **1-22, 26-30** and **34** are in a condition for allowance, which Applicant respectfully requests.

Applicant believes this Response should allow the Examiner to allow the above-referenced patent application to issue as a U.S. patent without further amendments to the specification or claims. Thus, Applicant also requests notification to that effect.

If questions should arise, please telephone the undersigned attorney.